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ABSTRACT

We report a superconducting kinetic inductance memory (SKIM) element, which can be controlled exclusively by the bias supercurrent, without involving magnetic fields and heating elements. The SKIM is nonvolatile memory. The device is made of two Nb Dayem bridges, and it can operate reliably up to 2.8 K. The achieved error rate is as low as one in 10^5 operations.

Superconducting supercomputers could provide a powerful alternative to modern semiconductor-based computers since the power dissipated in superconducting elements can be very low, i.e., it can approach thermodynamic and quantum information processing limits.[1,2] The "bottleneck" for the development of superconducting computers is the absence of a compact fully superconducting memory element.[1] Nanowires[3–8] provide an important alternative to the existing elements based on tunnel junctions[9–14] since their operation is based on their kinetic inductance,[1,3,15] which could be very large in nanowires with nanometer-scale dimensions. The employment of a large kinetic inductance for the memory function allows for a great reduction of the dimensions of the device.[1,3]

Previously reported superconducting memory elements either required magnetic fields for their functioning or were not fully superconducting since some of their elements required Joule heating.[3,4,16] Here, we report a fully superconducting kinetic inductance memory (SKIM) element, based on single quantized superconducting fluxons, which is expected to be free from previously existing drawbacks listed above. The SKIM is made of Nb, deposited over a pair of suspended SiN nanoconstrictions. The reported memory does not require sub-Kelvin temperatures, as was the case in many previously reported devices. Our SKIM element was tested in a cryogen free refrigerator and was operational up to a temperature of ∼3 K. The highest frequency of the memory switching, tested up to ∼50 kHz, was limited by the setup equipment and, in principle, could be much higher since the phase of the order parameter can change at a much higher rate.[17]

The sample geometry is shown in Fig. 1(a). The cross section is shown in Fig. 1(b), where the trench design is illustrated while the bridge is not shown. The top view is shown in Fig. 1(c). The sample contains two suspended nanobridges connected at each their end to thin superconducting films, which are referred to as "electrodes" or "leads." The electrodes and the nanoconstrictions are made of a 15-nm-thick Nb film. To fabricate the sample, a line-with-break pattern is prepared by e-beam lithography with a line dosage of 9 nC/cm on a 60 nm SiN/500 nm SiO_2/500 μm Si substrate. In each e-beam lithography session, we pattern a whole 4″ wafer with hundreds of pairs of SiN bridges,[21] which can be later used for metal deposition followed by photolithography patterning of the leads. Each device has its unique number markers (device numbers) near the nanobridges, such that we can tell them apart. The dimension of each nanobridge is a function of the device number. This design allows us to produce nanobridges of various sizes. We intentionally make multiple devices with the same device number and control the fabrication process so that devices with the same numbers always have very similar nanowire dimensions. This method allows us to make batches of samples with high reproducibility. The trench and nanobridges are developed in a 2 min 30 s SF6 reactive ion etching (RIE) and a 10 s HF wet etching, needed to form an undercut, to make the nanobridges suspended. The undercut is visible in Fig. 1(a) as a gray area on both sides of the trench. The resulting structure contains a 200-nm-wide trench [dark area in Fig. 1(a)] and two constrictions bridging the gap over the trench. The width of the SiN nanobridges is typically in the range of 10–30 nm. A 15 nm Nb film is sputtered over the SiN nanobridges to form superconducting nanoconstrictions, the width of which is defined by the width of the underlying SiN bridge. Initially, there are many nanobridges crossing the trench. We use photolithography to

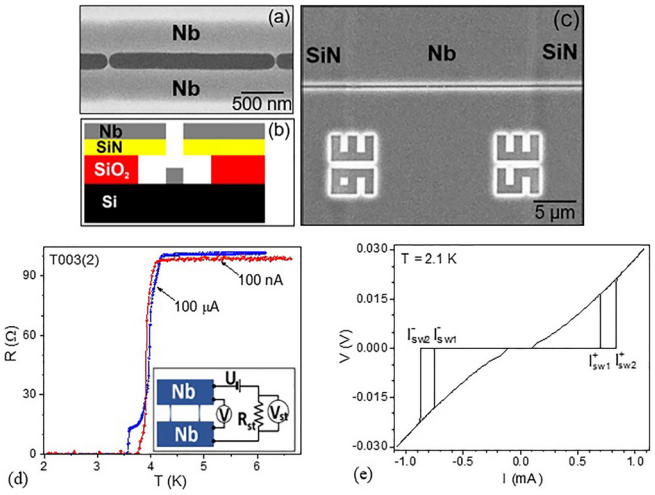

FIG. 1. (a) Scanning electron micrograph of the sample. The darkest gray area that runs through the middle of the image is the trench. The medium gray regions on both sides of the trench correspond to the undercut under the SiN layer, obtained by the HF etching during the fabrication. The light gray areas at the top and bottom of the image are areas of SiN with no undercut. Two Nb nanobridges connect the top Nb electrode and the bottom Nb electrode. The Nb electrodes are separated by a 200-nm-wide trench (black). The Nb nanobridges are suspended over the trench. (b) Cross-sectional schematic of the trench, undercut, and the Nb/SiN/SiO_2 multilayer deposited on a Si substrate. Not to scale. (c) The above SEM image is taken on a representative sample. It shows the trench (horizontal) and the Nb strip located between the two markers and extended perpendicular to the trench. Two nanowires are barely visible in the middle of the trench. (d) The sample resistance plotted vs the temperature. There are two curves, one (red) measured at a very low bias current (100 nA) and the other (blue) taken at a higher bias current (100 μA). The critical temperature is $T_C = 4$ K. (d, inset) Schematic of the memory element. The element contains a loop formed by the two bridges linked to two Nb electrodes. Such a superconducting loop can have different vorticity states and serves as a nonvolatile memory element, able to store one bit of information. (e) Multiple I-V curves are shown, measured at T = 2.1 K. Each current sweep exhibits only two switching currents, i.e., one positive and one negative. When multiple I-V curves are superimposed, collectively they show all possible switching currents, namely, two states at the positive branches (I^+_{sw1} and I^+_{sw2}) and two at the negative branches (I^-_{sw1} and I^-_{sw2}).

select and protect a pair of nearby nanoconstrictions and to define the electrodes. The unprotected Nb is removed by 2 min 30 s SF6 RIE.

The sample was placed in a cryogen-free cooler RDK-101DL (Sumitomo Heavy Industries, Ltd.) providing the base temperature of 2 K. The leads were thermalized by passing them through copper powder RF radiation filters, filled with a fixture of Stycast epoxy and Cu particles.[18]

The current bias of the sample was set by taking an ac voltage, U, from a high precision source DS360 and applying it to the sample connected in series with a standard resistor of $R_{st} = 1\,\text{k}\Omega$ [see Fig. 1(d), inset]. Such a circuit will be referred to as the "DS360 circuit." The sample resistance was much lower than the standard resistor. The lowest frequency was 10 Hz, low enough so that further reduction of the frequency would not change the shape of the voltage pulses. Yet it was possible to push the frequency up to 50 kHz and still obtain reliable reading of the memory states. The voltages on the sample, V, and on the resistor, V_{st}, were measured using National Instrument data acquisition card NI-DAQ USB-6216. The current in the circuit, I, was calculated as $I = V_{st}/R_{st}$. The voltages on the sample and the resistor were amplified using low noise differential preamplifiers SR560 Stanford Research Systems, before being supplied to the DAQ card. In some cases, a modified circuit was used, which will be called the "DAQ card circuit." This circuit is exactly the same as the "DS360 circuit," except that the voltage, needed to generate the bias current, was taken from the outputs of the same card NI-DAQ USB-6216. In the latter case, the experiment was controlled using Python code. In each measurement presented below, we will specify the type of the circuit and the frequency.

The temperature dependence of the resistance ($R = V/I$) of the sample is shown in Fig. 1(d). There are two curves on the graphs: one is taken at low bias current (the red curve), which does not impact the shape of the curve significantly, while the other (blue) is taken at a much higher current, which was smaller but of the same order as the critical current of the nanobridges. The first curve shows the true temperature dependence and confirms that nanobridges have the same critical temperature as the film. However, since they have a much lower critical current (since they are much narrower than the film), the curve taken at a higher bias current shows two transitions. This R-T curve shows that the normal resistance of the film was ~85 Ω and the normal resistance of the nanobridges was ~15 Ω. Taken the dimensions of the nanobridges (20 nm by 15 nm), we estimate the resistivity 9 $\mu\Omega$ cm, which is a typical value for the Nb thin film.[19]

The voltage vs current curve ("I-V curve") is shown in Fig. 1(e). It exhibits two different switching currents of the order of 1 mA (only one critical current is observed in each sweep though). There were two possible switching currents on the positive side, indicating that the system could be in two possible states. The same is true for the negative side of the I–V curve. The positive and negative switching currents were approximately equal but not exactly equal, i.e.,

$$|I^-_{sw1}| \approx |I^+_{sw1}| \quad \text{and} \quad |I^-_{sw2}| \approx |I^+_{sw2}|.$$

The origin of the two switching currents, as will be discussed later, is the possibility of different integer values of the winding number of the superconducting condensate wave function defined on the loop formed by the two nanobridges. This winding number will be used to store information. It should be emphasized that if the curve would be measured just one time, then it would show just one value of the critical current. Yet if the bias current is cycled many times, as is the case in Fig. 1(e), then the multivalued I-V curve, having two switching currents, emerges. The I-V curve also shows hysteresis, and the retrapping current appears much lower than the switching current. We explain this by Joule heating. Note that the voltage observed after the switching is of the order of 15 mV, which is in agreement with the normal resistance of the nanobridges estimated from the R-T curves (see above).

We have also tested the temperature dependence of the critical currents ("switching currents") [Fig. 2(a)]. It appears that the distinction between the two critical currents becomes smaller and almost disappears at ~3.2 K. Since the distinction between the critical currents will be used to determine the winding number of the loop, the temperature has to be substantially lower than ~3.2 K for the memory to function reliably.

The fluctuations of the switching current have also been measured [Fig. 2(b)]. It is clear that the standard deviation is of the order of 1 μA, which is much smaller than the difference between the two

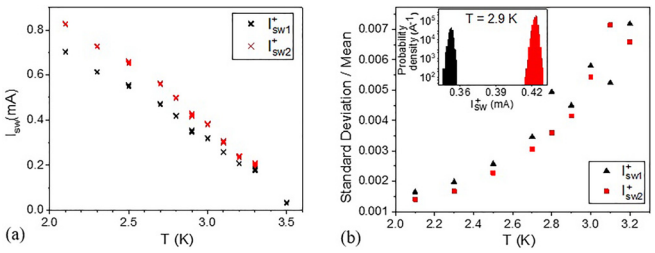

FIG. 2. (a) The two possible values (black and red) of the critical current ("switching current") plotted vs the temperature. (b) Dispersion of the switching current. The standard deviation is computed over an ensemble of 10 000 points. It is normalized by the mean value of the switching current. [(b), inset] Probability distribution of the switching current (T = 2.9 K). The total number of measurements was 10 000. Here, the "DS360 circuit" was used with the sweep frequency of 10 Hz. For the sinusoidal signal used here, the estimated sweep rate is ~40 mA/s.

critical currents (~0.1 mA). Thus, these fluctuations cannot cause the memory switch between the states.

Figure 3 shows the dependence of the switching current on the perpendicular magnetic field. The function is periodic and multivalued. Each branch of this periodic function represents a certain vorticity of the memory loop, or, in other words, the winding number of the order parameter, or, in other words, the number of fluxoids trapped in the loop.[3,6,22] This number will be denoted as n_v. The observed periodicity shows that vortices do not sit in the nanobridges themselves but enter the space between the bridges. Also, it shows that the vortices enter the loop in a periodic manner as the magnetic field is increased. The key observation is that the function is multivalued even at zero field. Thus, we conclude that two vorticity states are possible at zero field. These states can be used to store one bit of information. Below, we will discuss how to switch the system between the two stable vorticity states by the bias current, without applying external magnetic field. Generally speaking, this will be possible because a state with

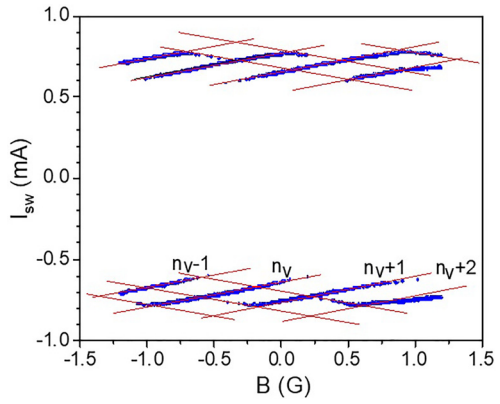

FIG. 3. Magnetic field dependence of the switching current (critical current). The multivalued nature of the switching current is clearly visible, representing different integer vorticity states of the loop, formed by the pair of parallel Nb nanobridges. The vorticity is indicated above each branch. Here, the "DAQ card circuit" was used with the time step of 100 ms.

a fixed number of vortices in the loop (n_v) has different positive and negative critical currents due to the fact that the bridges are not identical (asymmetry).

The reason that the switching current has two possible values at zero magnetic field is that the system can have vorticity zero ($n_v = 0$) or a unit vorticity ($n_v = 1$), which is realized if a vortex is trapped in the loop.[6] As the bias current is applied, it is added to the persistent current in the loop. Therefore, the observed switching current is lower in the case $n_v = 1$.

The main question is how to switch the system between the states without applying the external magnetic field. Our method is as follows. We apply a control current $I_0 = (I^+_{sw1} + I^+_{sw2})/2$ and measure the voltage. If the voltage is zero, that means $n_v = 0$. These memory states are considered logical zero (mem = **0**). If the voltage is not zero, then the bias current is reduced to zero and increased again to the value I_0. Again, if the voltage is zero, then the logical zero state is considered written (mem = **0**). This cycle is repeated until the voltage is zero when the current I_0 is applied. Since the process is stochastic, each time we apply current and reduce it to zero the probability that the desired state is established is roughly 50%. To test the effectiveness of this procedure, we have made 12 500 measurements. The results are shown in Fig. 4(a). The plot shows the distribution of the number of attempts needed for the creation of the state mem = **0** after the memory eraser. In 50% of cases mem = **0** obtains from the first attempt, in 25% of cases two attempts are needed, in 12.5% cases three attempts are needed, etc. Therefore, for example, if one requires a confidence of 10^{-6}, then one needs to cycle the current 20 times. If the frequency of the pulses would be set at a high value, say 10^{10} s^{-1}, then the time needed to create the desired memory state would be 5×10^{-8} s.

To write the state mem = **1,** a similar procedure is used, but the applied current is negative, namely, $I_1 = (I^-_{sw1} + I^-_{sw2})/2$. Note that here the switching currents are negative, $I^-_{sw1} < 0$ and $I^-_{sw2} < 0$.

To read out the state of the memory, we always apply the current $I_0 = (I^+_{sw1} + I^+_{sw2})/2$ and measure the voltage on the device. If the measured voltage is zero, then the state was mem = **0**; if the voltage is a few mV, then the state was mem = **1** before the measurement. The state is destroyed if mem = **1** is measured, since in this case, the system switches into the normal state and the order parameter is destroyed. By repeating the critical current measurement many times, we can plot distributions as shown in Figs. 4(b)–4(d). The top distribution [Fig. 4(b)] was measured without preparing the sample state in any way. Thus, a random sequence of the critical currents I^+_{sw1} and I^+_{sw2} was measured. The corresponding distribution (black) shows two peaks due to the fact that the sample can be found in two different vorticity states, n_v. Different vorticity states have different values of the persistent supercurrent. Thus, they impact differently on the critical current of the device.

Next, we perform a test in which the vorticity state is set to $n_v = 1$ (mem = **1**) before each measurement of the switching current. In this state, the system shows the lower critical current I^+_{sw1} at the positive bias and the higher critical current, I^-_{sw2}, at the negative bias. Note that $|I^-_{sw2}| > |I^+_{sw1}|$. The corresponding distribution, measured at positive bias currents, is shown by the red bars in Fig. 4(c). The distribution shown by the blue bars [Fig. 4(d)] was measured in a similar way, but the state of the memory was mem = **0** ($n_v = 0$) before each measurement of the switching current. The key observation from Figs. 4(b)–4(d) is that it is possible to select the desired state of the

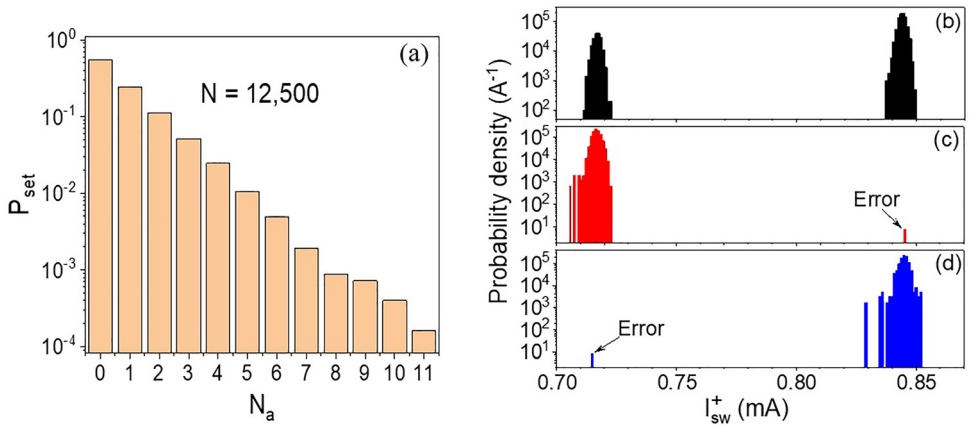

FIG. 4. The "DAQ card circuit" measurement with the time step of 100 ms. (a) The distribution of the number of attempts needed for the creation of the state mem = **0** after memory erasure. Here, $P_{set}(N_a)$ is the probability that the memory state is switched to mem = **0** after N_a attempts. [(b)–(d)] Probability distribution of the switching current (T = 2.1 K): (b) switching current of the unconditioned sample; (c) the sample was conditioned to mem = **1**, before each switching current measurement; and (d) the memory element was set to mem = **0** before each measurement. The total number of measurements used to plot each one of these three distributions was about 200 000. This figure shows that the memory, once written to successfully, can be read out with low error probability.

memory and the distribution becomes a well-defined single peak, with only one error out of about 200 000 measurements.

The measurement of Fig. 5(a) illustrates the operation of the memory. [Note that the plots in Fig. 5(c) represent a different algorithm, which will be explained later.] In Fig. 5(a), we first write the memory state, then read it out to verify that the state is still the same as was written. The sequence of written states was 0000–1111-0000–1111, etc. Let us remind that the term "write mem = **0**," here as always, means to cycle the bias current between zero and I_0 until we detect zero voltage at $I_0=(I^+_{sw1} + I^+_{sw2})/2$. Similarly, the term "write mem = **1**," here as always, means to cycle the bias current between zero and $I_1=(I_{sw1} + I_{sw2})/2 < 0$ until we detect zero voltage at I_1. After each state from the sequence was written, the memory state was read out. For the readout, the current was set to $I=I_0$ and the voltage was measured. It the voltage is zero, then mem = **0**, and if the voltage is high, then mem = **1**. (In the latter case, the reading procedure destroys the memory state.) Figure 5(a) clearly shows that the resulting sequence of readout states is exactly the same as the sequence of the written states. Within this example, a total of 25 write-read cycles is performed and no errors observed. If the test is continued for 100 000 write-read cycles, then we find a few errors. Thus, the error rate is of the order of 10^{-5}.

The two types of error rates (write-0-read-1 error rate, w**0**_r**1**, and write-1-read-0 error rate, w**1**_r**0**) were calculated by dividing the error number by the number of measurements [Table I; Fig. 5(b)]. The total error rate, Err_{tr}, is calculated by dividing the sum of the two types of errors by the total number of measurements, N, which was typically $N \sim 300\,000$.

At higher frequencies (~10 kHz), the "DS360 circuit" was used. The generator output was exactly periodic, i.e., no "read" and "write" algorithm defined above was possible when the generator DS360 was used. The error rates have been determined by applying a sequence of current-bias square pulses, switching between the positive limit I_0 and the negative limit $I_1 < 0$. The result is shown in Fig. 5(c). In this case, we show the voltage on the sample (red) and the voltage on the

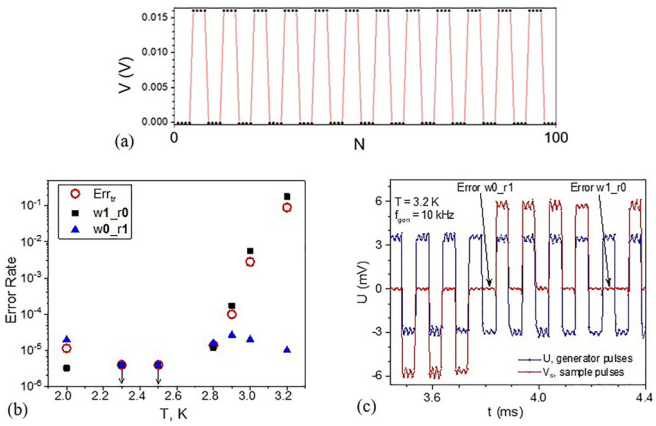

FIG. 5. (a) Slow measurement performed using "DAQ card circuit" with the time step of 100 ms. In this test run, we write mem = **0** state four times. After each writing, we read out the state and put a point on the plot, which is shown as the voltage on the device. Then, we write the mem = **1** state, also four times. After each such writing, the state is readout and the resulting voltage on the device is put as a point on the plot. Thus, we observe four mem = **0** states then four mem = **1** states then four mem = **0** states etc. No errors are observed. (b) Error analysis from the data obtained in (a). The error rates, w**0**_r**1**, w**1**_r**0**, and Err_{tr} = w**0**_r**1** + w**1**_r**0** are plotted vs the device temperatures. The data points having the arrows attached to them provide the top limit estimate for the error rate. The exact values are unknown since within N ~ 300 000 measurements no errors have been detected. The numbers of errors begin to increase at higher temperatures due to the higher rates of thermally activated phase slips. (c) High frequency measurement performed with the "DS360 circuit" circuit, the generator frequency being 10 kHz. The algorithm here is very different compared to (a) and (b): Here, the function generator outputs a periodic signal, so there is no assurance that after each pulse a particular predefined memory state is achieved. The method of the error analysis for this case is explained in the text.

TABLE I. Error rates for various temperatures. The "DAQ card circuit" was used with the time step of 100 ms.

Error Rate	$T = 2$K	$T = 2.3$K	$T = 2.5$K	$T = 2.8$K	$T = 2.9$K	$T = 3$K	$T = 3.2$K
Err_{tr}	1.1×10^{-5}	0	0	1.4×10^{-5}	1×10^{-4}	2.8×10^{-3}	8.8×10^{-2}
w**0**_r**1**	1.9×10^{-5}	0	0	1.6×10^{-5}	2.6×10^{-5}	2×10^{-5}	1×10^{-5}
w**1**_r**0**	3.2×10^{-6}	0	0	1.2×10^{-5}	1.7×10^{-5}	5.5×10^{-3}	0.18

standard resistor (blue) vs time. The current is proportional to the voltage on the standard resistor. In some cases, such circuit performs non-demolition measurements (when the detected voltage is zero), and only such measurements have been used as starting points of the error-evaluation cycles. More specifically, if the current was positive and the sample voltage was zero, the state was assumed mem = **0**. Then, the current switched to the negative bias. If the measured voltage was high, then it was concluded that mem = **0**, so, there is no error. If, on the other hand, the voltage remained zero even when the current changes its polarity to negative, then the readout value was mem = **1**, so we counted this event as an error event. Thus, we tested the error rate w**0**_r**1**. Analogously, the other error rate, w**1**_r**0**, was also tested. The resulting total error rate was 2.3×10^{-5} for the 10 kHz memory switching rate and 3.2×10^{-5} for the 50 kHz switching of the memory. In the latter case, the error was higher due to the top speed limit of the DAQ card.

The dissipated power, P, can be estimated as $P \sim (I^{+}_{sw1} + I^{+}_{sw2}) \cdot V/2$, i.e., a typical switching current multiplied by the voltage, V, occurring during the switching event, when the wire enters the normal state. The switching current depends on temperature, so the estimated power is different for different temperatures. Namely, $P \approx 5\,\mu$W at $T = 2.1$ K, and $P \approx 1\,\mu$W at $T = 3.2$ K. The dissipated energy can be estimated as the dissipated power divided by the number of switching events per second. At the maximum tested rate, $f = 50\,000$ s^{-1}, the energy per one switching event is, therefore, $E \sim P/f = 10^{-11}$ J at $T = 3.2$ K (taking into account that there are two switching events per cycle). The dissipated energy can be strongly reduced if narrower or much narrower voltage pulses are used in future realizations of such devices. Also, the switching current and correspondingly the dissipated energy can be further reduced if the bridges are made narrower.

The error rate in our devices is of the order of 10^{-5} or less. It is instructive to compare this to the commercial memory devices. For example, according to Ref. 20, the raw bit error rate (RBER) in new NAND flash memories was 10^{-9}–10^{-8}. After 10 000 cycles, the RBER increased to 10^{-7}–10^{-6}. These values represent the raw error rate. When an error correction was employed, the rate became much lower.[20] Our devices do not have any error correction mechanism, but it could be implemented in more advanced realizations. The advantage of the superconducting nanowire devices is that the RBER does not depend on the number of cycles, unlike in NAND memories.

In conclusion, we present a superconducting kinetic inductance memory ("SKIM element"), which can operate at temperatures as high as ∼2.8 K, in a cryogen free cooler. The SKIM element is made of only superconducting materials, containing no normal-metal dissipative elements or ferromagnetic inclusions. Our SKIM was tested at frequencies of up to ∼50 kHz, the frequency being limited by the setup. The SKIM memory shows a low error rate (∼10^{-5}). This nonvolatile memory device stores information in a form of single flux quanta. Thus, in principle, just one phase slip in one of the nanowires would be sufficient to switch the memory from one state to the other. Such a regime is not yet realized but could be achieved if very narrow current pulses are applied to the device. In the future, the system can be coupled to a microwave readout system, thus increasing the rate drastically. Our next goal is to integrate such elements into an array. For this, a horizontal array of "bitlines," composed of multiple chains of such memory elements, will be crossed by an array of "wordlines," which will be superconducting wires able to create magnetic fields. The current in a bitline will be set slightly below the critical current so it cannot switch by itself. Then, the switching will occur only at the crossing point of the current-biased wordline and the current biased bitline, where the magnetic field will help the cell to switch.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]M. Manheimer, https://iarpa.gov/index.php/research-programs/c3 for "Cryogenic computing complexity (C3) IARPA-BAA-13-05."
[2]K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-THz-clock-frequency digital systems," IEEE Trans. Appl. Supercond. **1**, 3–28 (1991).
[3]A. Murphy, D. V. Averin, and A. Bezryadin, "Nanoscale superconducting memory based on the kinetic inductance of asymmetric nanowire loops," New J. Phys. **19**, 063015 (2017).
[4]Q.-Y. Zhao, E. A. Toomey, B. A. Butters, A. N. McCaughan, A. E. Dane, S.-W. Nam, and K. K. Berggren, "A compact superconducting nanowire memory element operated by nanowire cryotrons," Supercond. Sci. Technol. **31**, 035009 (2018).
[5]A. N. McCaughan, E. Toomey, M. Schneider, K. K. Berggren, and S. W. Nam, "A kinetic-inductance-based superconducting memory element with shunting and sub-nanosecond write times," Supercond. Sci. Technol. **32**, 015005 (2019).
[6]S. Lee, Y. Jung, and R. Agarwal, "Highly scalable non-volatile and ultra-low-power phase-change nanowire memory," Nat. Nanotechnol. **2**, 626–630 (2007).
[7]L. Chen, L. Wu, Y. Wang, Y. Pan, D. Zhang, J. Zeng, X. Liu, L. Ma, W. Peng, Y. Wang, J. Ren, and Z. Wang, "Miniaturization of the superconducting memory cell via a three-dimensional Nb nano-superconducting quantum interference device," ACS Nano **14**(9), 11002–11008 (2020).
[8]A. Murphy and A. Bezryadin, "Asymmetric nanowire SQUID: Linear current-phase relation, stochastic switching, and symmetries," Phys. Rev. B **96**, 094507 (2017).
[9]I. V. Vernik, V. V. Bol'ginov, S. V. Bakurskiy, A. A. Golubov, M. Yu. Kupriyanov, V. V. Ryazanov, and O. A. Mukhanov, "Magnetic Josephson junctions with superconducting interlayer for cryogenic memory," IEEE Trans. Appl. Supercond. **23**(3), 1701208–1701208 (2013).

[10]V. V. Ryazanov, V. V. Bol'ginov, D. S. Sobanin, I. V. Vernik, S. K. Tolpygo, A. M. Kadin, and O. A. Mukhanov, "Magnetic Josephson junction technology for digital and memory applications," Phys. Procedia **36**, 35–41 (2012).
[11]C. Guarcello, P. Solinas, M. D. Ventra, and F. Giazotto, "Solitonic Josephson-based meminductive systems," Sci. Rep. **7**, 46736 (2017).
[12]E. Goldobin, H. Sickinger, M. Weides, N. Ruppelt, H. Kohlstedt, R. Kleiner, and D. Koelle, "Memory cell based on a φ Josephson junction," Appl. Phys. Lett. **102**, 242602 (2013).
[13]B. M. Niedzielski, E. C. Gingrich, R. Loloee, W. P. Pratt, and N. O. Birge, "S/F/S Josephson junctions with single-domain ferromagnets for memory applications," Supercond. Sci. Technol. **28**, 085012 (2015).
[14]R. Caruso, D. Massarotti, A. Miano, V. V. Bolginov, A. B. Hamida, L. N. Karelina, G. Campagnano, I. V. Vernik, F. Tafuri, V. V. Ryazanov, O. A. Mukhanov, and G. P. Pepe, "Properties of ferromagnetic Josephson junctions for memory applications," IEEE Trans. Appl. Supercond. **28**(7), 1–6 (2018).
[15]F. Friedrich, P. Winkel, K. Borisov, H. Seeger, C. Sürgers, I. M. Pop, and W. Wernsdorfer, "Onset of phase diffusion in high kinetic inductance granular aluminum microSQUIDs," Supercond. Sci. Technol. **32**, 125008 (2019).
[16]B. A. Butters, "Development of a scalable superconducting memory," Master's thesis (Massachusetts Institute of Technology, 2018).
[17]T. Aref, A. Levchenko, V. Vakaryuk, and A. Bezryadin, "Quantitative analysis of quantum phase slips in superconducting Mo76Ge24 nanowires revealed by switching-current statistics," Phys. Rev. B **86**, 024507 (2012).
[18]J. M. Martinis, M. H. Devoret, and J. Clarke, "Experimental tests for the quantum behavior of a macroscopic degree of freedom: The phase difference across a Josephson junction," Phys. Rev. B **35**, 4682 (1987).
[19]O. V. Dobrovolskiy, E. Begun, M. Huth, and V. A. Shklovskij, "Electrical transport and pinning properties of Nb thin films patterned with focused ion beam-milled washboard nanostructures," New J. Phys. **14**, 113027 (2012).
[20]N. Mielke, T. Marquart, N. Wu, J. Kessenich, H. Belgal, E. Schares, F. Trivedi, E. Goodness, and L. R. Nevill, "Bit error rate in NAND flash memories," in 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ (2008), pp. 9–19.
[21]S. L. Chu, A. T. Bollinger, and A. Bezryadin, Phys. Rev. B **70**, 214506 (2004).
[22]A. Belkin, M. Brenner, T. Aref, J. Ku, and A. Bezryadin, Appl. Phys. Lett. **98**, 242504 (2011).